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09/846,119	04/30/2001	Yitzhak Gilboa	5298-04700 PM00028	5235

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EXAMINER	
GOUDREAU, GEORGE A	

ART UNIT	PAPER NUMBER
1763	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

1 D

Office Action Summary

Application No.	Applicant(s)
09-846,119	Gilboa et al.
Examiner	**Group Art Unit**
George Goudreau	1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 4-01-(ie, - paper # 1)

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-30 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-30 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (c) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

16. Claims 12-14, 17-18, and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Atsushi (JP 11-177,058).

Atsushi discloses a two step process for planarizing, and etching a BPSG layer (13) until an underlying SiO2 or Si3N4 layer (12) is reached during the formation of an ILD layer (12-13) on the surface of a wafer. The BPSG is cmp polished to planarize the surface during the first step. The planar BPSG layer is then etched back in a plasma comprised of (CHF3-CF4-Ar) until layer 12 of the ILD dielectric is reached which functions as a type of etch stop. This is discussed specifically in the abstract; and discussed in general in columns 1-16. This is shown in figures 1-9.

17. Claims 12-14, 17-18, and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et. al. (6,265,315).

Lee et. al. disclose a two step process for planarizing, and etching SiO2 layer (18) until an underlying Si3N4 layer (16) is reached during the formation of an ILD layer (14, 16, 18) on the surface of a wafer. The SiO2 layer is cmp polished to planarize the surface during the first step. The planar SiO2 layer is then etched back in a plasma comprised of (C4F8-CO-Ar) until the layer

16 of the ILD layer is reached which functions as a type of etch stop. This is discussed specifically in columns 3-5; and discussed in general in columns 1-8. This is shown in figures 1-8.

18. Claims 1-2, 5-6, 12-14, 19, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et. al. (6,063,689).

Chen et. al. disclose a process for forming an STI structure (124) on the surface of a wafer (100) which is comprised of the following steps:

-A bilayer mask (102, 104) is formed onto the surface of the Si wafer. Layer 102 is comprised of a pad SiO2 layer. Layer 104 is comprised of Si3N4. The bilayer mask is then patterned to form an etch mask.;

-The bilayer etch mask is then used in the etching of a trench in the Si wafer (100).;

-A SiO2 layer (116) is used to planarize the surface of the wafer as well as to fill the trench etched into the Si wafer.;

-The SiO2 layer (116) is then planarized, and etched using a two step process. During the first step, the SiO2 layer is cmp polished to planarize it. The planar SiO2 layer is then etched back in a plasma until the surface of the polysi layer (104) is reached which functions as a type of etch stop.; and

-The polysi, and SiO2 etch mask is then removed from the surface of the wafer using an etching process to leave behind an STI structure on the surface of the wafer.

This is discussed specifically in columns 3-4; and discussed in general in columns 1-6. This is shown in figures 1-2.

19. Claims 1-2, 5, 12-14, and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et. al. (6,136,713).

Chen et. al. disclose a process for forming an STI structure (206 b) on the surface of a wafer (200) which is comprised of the following steps:

-A Si3N4 etch mask (202) is formed onto the surface of the Si wafer.;

-The Si3N4 etch mask is then used in the etching of a trench in the Si wafer (200).;

-A SiO2 layer (206) is used to planarize the surface of the wafer as well as to fill the trench etched into the Si wafer.; and

-The SiO2 layer (206) is then planarized, and etched using a two step process. During the first step, the SiO2 layer is cmp polished to planarize it. The planar SiO2 layer is then etched back in a plasma until the surface of the Si3N4 layer (202) is reached which functions as a type of etch stop.

This is discussed specifically in columns 3-4; and discussed in general in columns 1-6. This is shown in figures 1-2.

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

22. Claims 3-4, 6-11, 15-16, 22-27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et. al. as applied in paragraph 19 above.

Chen et. al. as applied in paragraph 19 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a fixed abrasive pad, and a cmp slurry which contains no free floating abrasive particles to cmp polishing the surface of the SiO2 layer in the process taught above;

-the reduction of the thickness of the SiO2 fill layer to the specific thicknesses which are claimed by the applicant in the cmp polishing step;

-the formation of the Si3N4 etch mask layer to the specific thicknesses which are claimed by the applicant; and

-the specific formation of the etch mask layer used to form the trench in the Si wafer out of any of an oxide, a doped oxide such as BPSG, SiC, or a carbonated polymer

It would have been obvious to one skilled in the art to form the etch mask used in the etching of the STI trench in the Si wafer in the process taught above out of any of an oxide, a doped oxide such as BPSG, SiC, or a carbonated polymer based upon the following. The usage of these materials to form an etch mask on a Si wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming an etching mask on the Si wafer to those means which are specifically taught above.

It would have been obvious to one skilled in the art to employ a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles to conduct the cmp polishing step in the process taught above based upon the following. The conduction of a cmp polishing process using a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles is a conventional or at least well known means for conducting a cmp polishing process in the semiconductor arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for conducting the cmp polishing step in the process taught above to those means which are specifically taught above.

It would have been obvious to one skilled in the art to cmp polish the SiO2 layer in the process taught above until the thickness is reduced to the specific thicknesses which are claimed by the applicant base upon the following. It would have been obvious to one skilled in the art to use the cmp polish step to a sufficient extent to adequately, and rapidly planarize the surface of

the SiO2 layer without undesirably exposing the surface of the underlying layer based upon the teachings in this reference regarding these matters.

It would have been obvious to one skilled in the art to form the Si3N4 etch mask in the process taught above to the specific thicknesses which are claimed by the applicant based upon the following. It would have been obvious to one skilled in the art to form adequate thickness to the Si3N4 layer in the process taught above such that an adequate level of protection is provided to the underlying layers during each etching step without forming an inordinately thick layer of material which would adversely effect processing costs, and processing times for fabricating the device.

23. Claims 3-4, 7-11, 15-16, 20, 22-27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et. al. as applied in paragraph 18 above.

Chen et. al. as applied in paragraph 18 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a fixed abrasive pad, and a cmp slurry which contains no free floating abrasive particles to cmp polishing the surface of the SiO2 layer in the process taught above;

-the reduction of the thickness of the SiO2 fill layer to the specific thicknesses which are claimed by the applicant in the cmp polishing step;

-the specific formation of the etch mask layer used to form the trench in the Si wafer out of any of an oxide, a doped oxide such as BPSG, Si3N4, SiC, or a carbonated polymer; and

-the formation of the Si3N4 etch mask layer to the specific thicknesses which are claimed by the applicant

It would have been obvious to one skilled in the art to form the etch mask used in the etching of the STI trench in the Si wafer in the process taught above out of any of Si3N4, an oxide, a doped oxide such as BPSG, SiC, or a carbonated polymer based upon the following. The usage of these materials to form an etch mask on a Si wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming an etching mask on the Si wafer to those means which are specifically taught above.

It would have been obvious to one skilled in the art to employ a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles to conduct the cmp polishing step in the process taught above based upon the following. The conduction of a cmp polishing process using a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles is a conventional or at least well known means for conducting a cmp polishing process in the semiconductor arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means

for conducting the cmp polishing step in the process taught above to those means which are specifically taught above.

It would have been obvious to one skilled in the art to cmp polish the SiO2 layer in the process taught above until the thickness is reduced to the specific thicknesses which are claimed by the applicant base upon the following. It would have been obvious to one skilled in the art to use the cmp polish step to a sufficient extent to adequately, and rapidly planarize the surface of the SiO2 layer without undesirably exposing the surface of the underlying layer based upon the teachings in this reference regarding these matters.

It would have been obvious to one skilled in the art to form the Si3N4 etch mask in the process taught above to the specific thicknesses which are claimed by the applicant based upon the following. It would have been obvious to one skilled in the art to form adequate thickness to the Si3N4 layer in the process taught above such that an adequate level of protection is provided to the underlying layers during each etching step without forming an inordinately thick layer of material which would adversely effect processing costs, and processing times for fabricating the device.

24. Claims 15-16, 22-26, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et. al. as applied in paragraph 17 above.

Lee et. al. as applied in paragraph 17 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a fixed abrasive pad, and a cmp slurry which contains no free floating abrasive particles to cmp polishing the surface of the SiO2 layer in the process taught above; and

-the reduction of the thickness of the SiO2 fill layer to the specific thicknesses which are claimed by the applicant in the cmp polishing step

It would have been obvious to one skilled in the art to employ a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles to conduct the cmp polishing step in the process taught above based upon the following. The conduction of a cmp polishing process using a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles is a conventional or at least well known means for conducting a cmp polishing process in the semiconductor arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for conducting the cmp polishing step in the process taught above to those means which are specifically taught above.

It would have been obvious to one skilled in the art to cmp polish the SiO2 layer in the process taught above until the thickness is reduced to the specific thicknesses which are claimed

by the applicant base upon the following. It would have been obvious to one skilled in the art to use the cmp polish step to a sufficient extent to adequately, and rapidly planarize the surface of the SiO2 layer without undesirably exposing the surface of the underlying layer based upon the teachings in this reference regarding these matters.

25. Claims 5-16, 22-26, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi as applied in paragraph 16 above.

Atsushi as applied in paragraph 16 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a fixed abrasive pad, and a cmp slurry which contains no free floating abrasive particles to cmp polishing the surface of the SiO2 layer in the process taught above; and

-the reduction of the thickness of the SiO2 fill layer to the specific thicknesses which are claimed by the applicant in the cmp polishing step

It would have been obvious to one skilled in the art to employ a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles to conduct the cmp polishing step in the process taught above based upon the following. The conduction of a cmp polishing process using a fixed abrasive pad in combination with a cmp slurry which contains no free floating abrasive particles is a conventional or at least well known means for conducting a cmp polishing process in the semiconductor arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means

for conducting the cmp polishing step in the process taught above to those means which are specifically taught above.

It would have been obvious to one skilled in the art to cmp polish the SiO2 layer in the process taught above until the thickness is reduced to the specific thicknesses which are claimed by the applicant base upon the following. It would have been obvious to one skilled in the art to use the cmp polish step to a sufficient extent to adequately, and rapidly planarize the surface of the SiO2 layer without undesirably exposing the surface of the underlying layer based upon the teachings in this reference regarding these matters.

26. Claims 20-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

-The wording used in claims 20-21 is confusing, and should be reworded. The examiner is uncertain what type of structure the applicant is trying to claim in these claims.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag

Primary Examiner

AU 1763